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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/657,482	09/08/00	HARARI E	HARI.A06US3

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EXAMINER	
HUA, L	
ART UNIT	**PAPER NUMBER**
2131	3

DATE MAILED: 09/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/657,482	Harari et al.
Examiner	**Art Unit**
Ly V. Hua	2131

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____

2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *56-62* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *56-62* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Sep 8, 2000* is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

1. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore the following elements must be shown or the feature canceled from the claims:

a. the "standard power supply" recited in claim 56,
b. the "individually addressable storage cells" recited in claim 56,
c. the "spare storage cells" recited in claim 56
d. the "means for erasing" recited in claim 56,
e. the "means for reading" recited in claim 56,
f. the "means for programming" recited in claim 56, and
g. the "means for substituting" recited in claim 56;
h. the "means for initially programming" recited in claim 57,
i. the "means for initially determining" recited in claim 57, and
j. the "means for writing" recited in claim 57;
k. the "spare sectors" recited in claim 58;
l. the "means for performing error correction" recited in claim 59;
m. the "standard magnetic disk drive storage system" recited in claim 60;
n. the "means for operating" recited in claim 61, and
o. the "standard power supply" recited in claim 61; and
p. the "means for generating voltages" recited in claim 62,
q. the "means for error correction" recited in claim 62, and
r. the "storage system" recited in claim 62.

The applicant is requested to be consistent in usage of terminology so that terms used in claims can be readily seen in the drawings. No new matter should be entered.

2. Applicant is required to submit a proposed drawing correction in response to this Office action.

3. Claim 58 is objected to because of the following informalities:

a. **In claim 58:**
   i. At line 6, it appears that the word "sector" should be changed to --sectors--.

Appropriate correction is required.

4. Claims 57, 59, 60 and 62 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. **As per claim 57:**
   At lines 5 and 10, the phrase "said EEPROM memory" lacks antecedent basis.
b. **As per claim 59:**
   This claim is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2173.05(l). The Connections for the means for performing error correction have not been recited and thus its cooperation with other elements is considered incomplete.
c. **As per claim 60:**
   i. , It is not clear how the controller and the interface are connected to the system bus. It is not clear whether both the controller and the interface are directly connected to the system bus, the controller connected to the interface then the interface is connected to the system bus or the interface is connected to the controller then the controller is connected to the system bus.
   ii. At line 6, "said disk drive system" lacks proper antecedent basis.
d. **As per claim 62:**
   i. At lines 3 and 5, the phrase "the operation" lacks antecedent basis because the EEprom chips might have various operations and it is not clear which one of the various operations is referred to by the phrase.

ii. At lines 7, the phrase "the operation" lacks antecedent basis because the storage system might have various operations and it is not clear which one of the various operations is referred to by the phrase.

5. Claim 62 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The previous claim 56 claims a memory card; but claim 62 claims a storage system. Since claim 62 claims a different invention, claim 62 does not further limit the subject matter of the previous claim.

6. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

8. Claims 56 and 58 are rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474, hereafter referred to as Fukushi) in view of Rao (4,949,309) and common practices in the art.

a. <u>As per claims 56 and 58:</u>

i. Fukushi discloses the memory device substantially as claimed including means for substituting spare storage cells for storage cells that cannot be addressed.
Fukushi's storage cells are organized into a plurality of groups (or sectors) each of which contains a plurality of storage cells.
It is inherent that the disclosure of Fukushi is associated with a computer system which is connected to a system bus lines which are connected to the memory device.

ii. However, Fukushi's memory device does not show:
(a) a plurality of chips of EEPROM type.
This is because:
(1) Fukushi's regular and spare memory cells are of general type and are not limited to EEPROM type and
(2) those cells are plentiful enough that a plurality of the combination of Fukushi's elements 1 and 7 and memory expansion are not necessary.

iii. Rao teaches:
(1) a plurality of EEPROM memory cells which are partitioned into groups (or sectors) each of which groups comprises

(a) a plurality of storage cells that can be individually addressed for individually programming and erasing each of the storage cells without disturbing the other storage cells.

iv. Official Notice is, hereby, taken that:

(1) it is a common practice in the art to provide a memory device (such as an EEprom) with the necessary means such as:

(a) means for erasing memory cells,

(b) means for programming memory cells, and

(c) means for reading the content of memory cells; and

(2) it is a common practice in the art to add memory chips to increase memory size.

v. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(1) apply

(a) both

1) Fukushi's teaching of substituting spare storage cells for regular storage cells and

2) Rao's teaching of using EEPROM cells as a storage cells

(i) to design memory device having Rao's EEPROM cells and

(b) Fukushi's means for substituting spare storage cells for regular storage cell.

vi. The person having ordinary skill in the art would have been motivated to combine the teachings of Rao and Fukushi **because** :

(1) the person would wish to substitute a spare storage cell for a regular storage cell when the regular storage cell cannot be acted on as taught by Fukushi and

(2) that person would know that EEPROM cells are like any other kind of memory cells are some time cannot be acted on (due to defect).

b. As per claim 61:

i. Official notice is taken that it is a common practice in the to provide various operating voltages for operating the various operations on an EEPROM and it is also a common practice in the art to provide a necessary voltage regulating means for generating various operating voltages from a power supply to supply the various operating voltages to operate the EEPROM.

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide various EEPROM operating voltages to various operations of an EEPROM **because** the various operations of the EEPROM do require various operating voltages.

c. As per claim 57:

i. Official notice is taken that transferring data to a memory device through a cache is a common practice in the art.

ii. It would have been obvious to one having ordinary skill in the art at the time the invention was made to write data to a cache prior to write it into a memory device because in this way the memory device might be slow at it writing operation and because the source which sends the data cannot afford to wait.

iii. The person having ordinary skill in the art would have been motivated to write data to a cache prior to writing it to a memory device because it would enhance processing time efficiency at the source which sends the data.

9. Claim 59 is rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474) hereafter referred to as Fukushi), Rao (4,949,309) and common practice in the art as applied to claims 56 and 58 above and further in view of Takemae (4,688,219).

As per claim 59:

i. Takemae teaches:
   (1) a means for correcting those error which can be corrected by using error correction codes.

ii. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Takemae with the teachings of Rao and Fukushi to add an error correction means into the obvious memory device which has been addressed above in the rejection of claim 56 and 58.

iii. One having ordinary skill in the art would have been motivated to add, in addition to the means for substituting spare bits for faulty regular bits, an error correction circuit to a memory card **because** one would consider a situation of soft error as taught by Takemae.

10. Claim 60 is rejected under 35 U.S.C. § 103 as being unpatentable over Fukushi et al. (4,757,474) hereafter referred to as Fukushi), Rao (4,949,309) and common practice in the art as applied to claim 56 above and further in view of Tuma et al (5,070,474 hereinafter referred to as Tuma).

As per claim 60:

i. A controller (i.e., the SMD disk controller, which see a solid state memory as a disk), which is interfaced with a solid state memory, for responding to commands sending to a disk and for controlling the solid state memory (col. 4, lines 9-37).

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Tuma's controller to the modified memory device of Fukushi.

iii. The artisan would have been motivated to add Tuma's controller to the modified memory device of Fukushi because:
   (1) Fukushi's memory device is of solid state type;
   (2) Tuma's memory is of solid state type; and
   (3) The addressing of the solid state memory of Fukushi is similar to the addressing of the solid state memory of Tuma as it is expected in the art of addressing solid state memories.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703)305-9724 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gail Hayes, can be reached on (703) 305-9711. The fax phone number for this Group is (703) 305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

LY V. HUA
PATENT EXAMINER
ART UNIT 2131

L. Hua
September 10, 2001